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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/332,726	06/14/1999	PAUL STEPHAN BEDROSIAN	7	3263

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EXAMINER	
GEORGE, KEITH M	
ART UNIT	**PAPER NUMBER**
2663	12

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/332,726	Applicant(s) BEDROSIAN, PAUL STEPHAN	
	Examiner Keith M. George	Art Unit 2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 9 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itri, U.S. Patent 5,864,592, hereinafter Itri.

3. Referring to claims 1, 9 and 17, Itri teaches a timing recovery system for digital subscriber line transceivers. This system, described in reference to figure 5, contains a master timing source (figure 5, master clock) (external timing reference) supplied by the central office and the remote terminal (receiver) derives the timing information from the received signal (transmitter generating a digital subscriber line transport signal including frequency and phase information) (column 1, lines 28-50 and column 5, lines 27-44). It is also clearly taught in figure 5 that a command signal (depicted by dashed line 208) representing the phase error detected by detector 206, is communicated via transceiver 3 transmitter over channel 1 (preferably within a frame overhead field) (a payload signal and a transmitter-side timing reference signal) (column 5, lines 30-34). Itri also teaches in more detail in figures 4A and 4B the phase control block taught in figure 3. The phase control circuit in figure 4A contains a numerically controlled oscillator (120) that should be considered as a specific type of phase adjust circuit whose function is analogous to the phase adjust circuit 100 of Figure 4B (local oscillator in the

transmitter adapted to receive the transmitter-side timing reference signal as an external timing reference) (column 4, lines 35-42). Itri teaches all of these components in block diagram form and possibly fails to teach that the phase adjust and phase error detect blocks shown in figure 5 are part of the transmitter. However, one of ordinary skill in the art would clearly understand that the left side of figure 5 is the central office station and all of the components under that heading can be grouped together as the "transmitter". One of ordinary skill in the art would be motivated to do this because individual blocks of block diagrams are commonly used in the art to represent different functions but do not necessarily represent separate components.

4. Referring to claims 2, 3, 5, 10, 11, 13 18, 19 and 21, Itri teaches the system described in reference to claims 1, 9 and 17 above and also clearly teaches that in a High Bit-Rate Digital Subscriber Line (HDSL) system, a 1.544 Mbit/sec T-1 (DS1) data stream is transmitted over two channels each operating at a rate of 784 Kbit/sec (column 1, lines 19-22). It is clear from the remaining teachings of Itri that one of the intended uses of the invention is to operate in an HDSL system as described.

5. Referring to claims 6, 14 and 22, Itri teaches the system described in reference to claims 1, 9 and 17 above and also clearly teaches that a phase error detector detects the phase error and a command signal representing the phase error detected (synchronization status message) is communicated to a phase adjust circuit (column 5, lines 27-35).

6. Claims 4, 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itri in view of Near et al., U.S. Patent 5,068,877, hereinafter Near. Itri teaches the system described in reference to claims 1 and 9 above with the possible exception of using stratum 1 traceable synchronization information. Near teaches a method for synchronizing interconnected digital

equipment and further teaches the basic concept of the stratum level. The stratum level refers to four defined levels of clock performance (1 through 4) as defined in standards documents such as in ANSI T1.101-1987. Smaller stratum level numbers represent more accurate timing performance. Particularly, a stratum 1 clock occupies the highest level in the synchronization hierarchy and is known as the frequency reference (common time base) for the entire synchronization network. It is a primary frequency standard with a minimum accuracy defined to be better than 1×10^{-11}. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a master clock at the highest stratum level (master clock in figure 5 of Itri) (Near, column 2, lines 25-26). One of ordinary skill in the art would have been motivated to use a stratum 1 timing reference as taught by Near would help to avoid timing or synchronization errors. Typical problems resulting from timing or synchronization errors can vary from exchange of incorrect or incomplete information to complete blockage and communication failure of the network (Near, column 1, lines 50-53).

7. Claims 7, 8, 15 and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Itri in view of Narasimha et al., U.S. Patent 5,638,379, hereinafter Narasimha. Itri teaches the system described in reference to claims 1 and 9 above with the possible exception of a timing reference signal generated by a building integrated timing supply having GPS capability and a transmitted clock is generated by an add-drop multiplexer associated with the transmitter. Narasimha teaches that in a digital network, there is a plurality of primary reference source checks implemented using GPS receiver technology (column 1, lines 30-34). Narasimha also teaches that the frame start signal and the line clock can be obtained from an add-drop multiplexer (column 4, lines 18-20). At the time the invention was made, it would have been obvious to a

person of ordinary skill in the art to utilize the GPS and ADM teachings of Narasimha in the system of Itri. One of ordinary skill in the art would have been motivated to do this because in a typical digital network, there area plurality of primary reference source checks called PRS checks. Typically, the PRS clocks are implemented using cesium beam or GPS receiver technology. The PRS clocks serve as master clocks and provide a timing reference for the remainder of the network (Narasimha, column 1, lines 30-35).

Response to Arguments

8. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Eldering et al., U.S. Patent 6,704,930, teaches that a synchronization manger provides a reference clock and in an exemplary case, the reference clock is a stratum 3 network clock.

b. Czerwiec, U.S. Patent 5,640,512, teaches that if network synchronization is required, it must be assumed that the connecting equipment has stratum clock traceability from a separate source.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith M. George whose telephone number is 703-305-6531. The examiner can normally be reached on M-Th 7:00-4:30, alternate F 7:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 703-308-5340. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Keith M. George
22 June 2004

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 6/23/04